ZedBoard Rev D.2 Errata

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1 Introduction

Thank you for your interest in the ZedBoard. Although Avnet and Digilent have made every effort to ensure the highest possible quality, these kits and associated software are subject to the limitations described in this errata notification.

Be aware that any of the optional workarounds requiring physical modifications to the board are done at the User's own risk. Neither Avnet nor Digilent is liable for any user performed rework.

2 Identifying Affected Kits

The kits affected by these errata are Revision D.2. Kits can be identified by the Revision of the ZedBoard in the kit and the additional pictures provided in the explanations below. The Revision of the ZedBoard can be found just below the barcode.

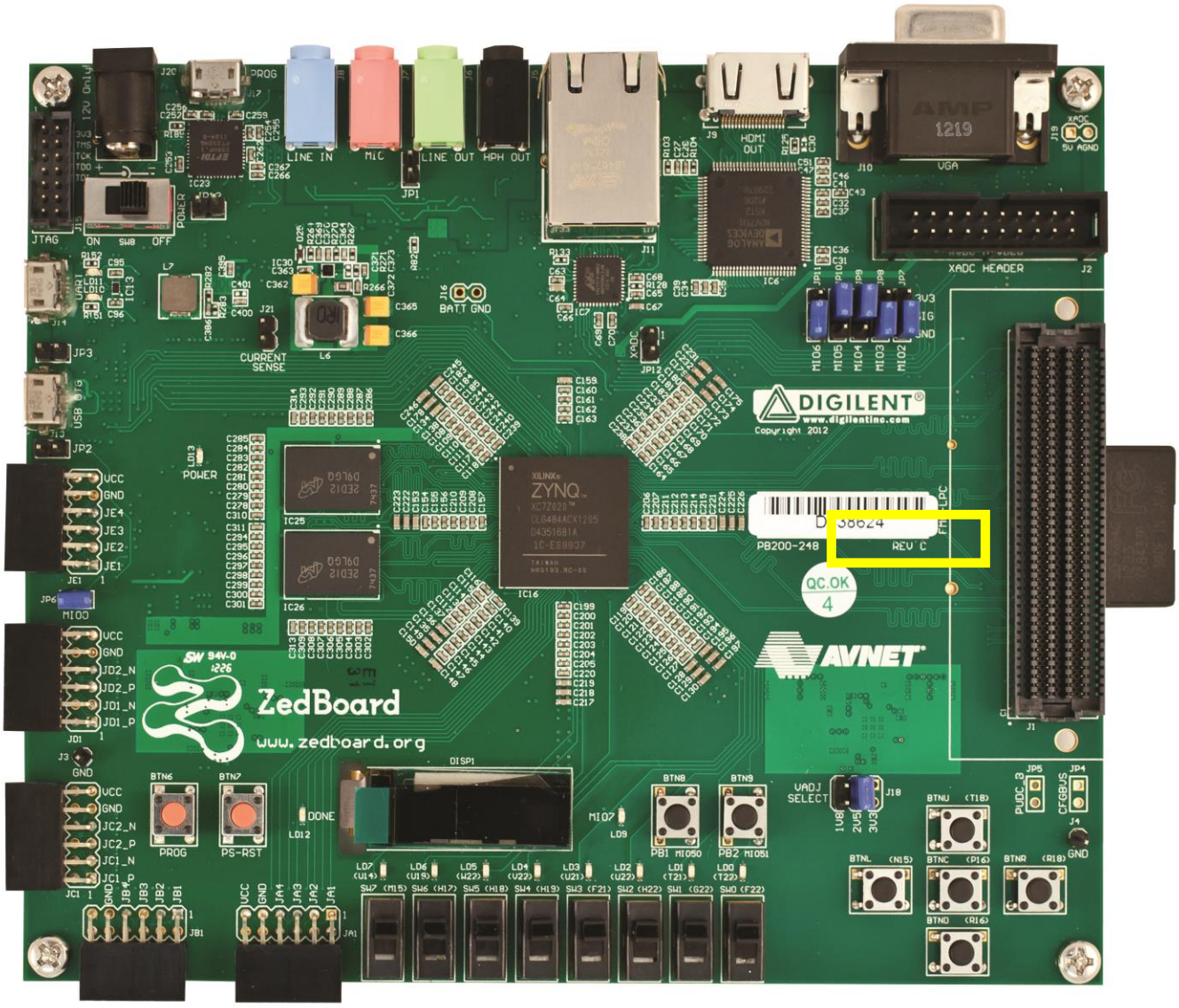

Figure 1 – Identifying ZedBoard Revision (Rev C shown – this errata covers Rev D)

3 Errata

3.1 Zynq Applications Fail Due to Heat

Applications Affected

Designs that exercise the Zynq on the ZedBoard at the highest performance (especially FMC card applications) or high ambient temperatures may experience a heat-related failure. Similar applications may not fail on the ZC702, which has the same 7z020 device.

Description

The Rev D ZedBoard ships with a Commercial temperature grade Zynq device. According to the Zynq datasheet, the maximum operating junction temperature is specified at 85° C. When the junction temperature exceeds 85° C, the Zynq device may experience failures.

Table 2: **Recommended Operating Conditions(1) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

The Zynq junction temperature is a function of the ambient temperature, internally generated heat due to operation, and the ability of the Zynq package and ZedBoard PCB to dissipate that heat. Applications that utilize the Zynq at higher operating frequencies or fuller capacity or more I/O will consume more power and thus generate more heat. Applications that make use of an FMC may be particularly susceptible to more heat due to the extra logic and I/Os to interface to the card. In some cases, the ZedBoard Zynq Tj may exceed 85° C and fail. ChipScope was used to access the XADC to measure Tj and verify that Tj did exceed 85° C during demanding applications.

Given the same Zynq application with FMC running under similar conditions, field failures have occurred on ZedBoard that do not occur on ZC702. This is attributed to the ZC702's better ability to dissipate heat. The ZedBoard was designed to be lower cost. For this reason, several cost-cutting measures were taken related to the PCB, outlined below. The trade-off for these decisions is ZedBoard's decreased capacity to dissipate heat out of the Zynq device in demanding applications.

- Thinner dielectric layers
- Fewer copper plane (power and ground) layers
- Fewer total layers
- Reduced copper thickness

For these reasons, ZedBoard may be susceptible to heat-related failures with demanding applications, especially applications utilizing FMC. High ambient temperatures may also cause problems with ZedBoard.

Workaround

A heatsink applied to the ZedBoard's Zynq device is recommended for all applications. All Rev D ZedBoards are populated with a CTS BDN09-3CB/A01 passive heatsink. Additionally, the most demanding applications will benefit from a fan to produce airflow over the ZedBoard. For example, the Zynq-7000 SoC / Analog Devices Software-Defined Radio Kit will ship with Sunon fan UF3H3-700, which can be operated from 3.3V power available through one of the Pmod connectors.

Both the heatsink and the fan are listed on the ZedBoard Accessories page.

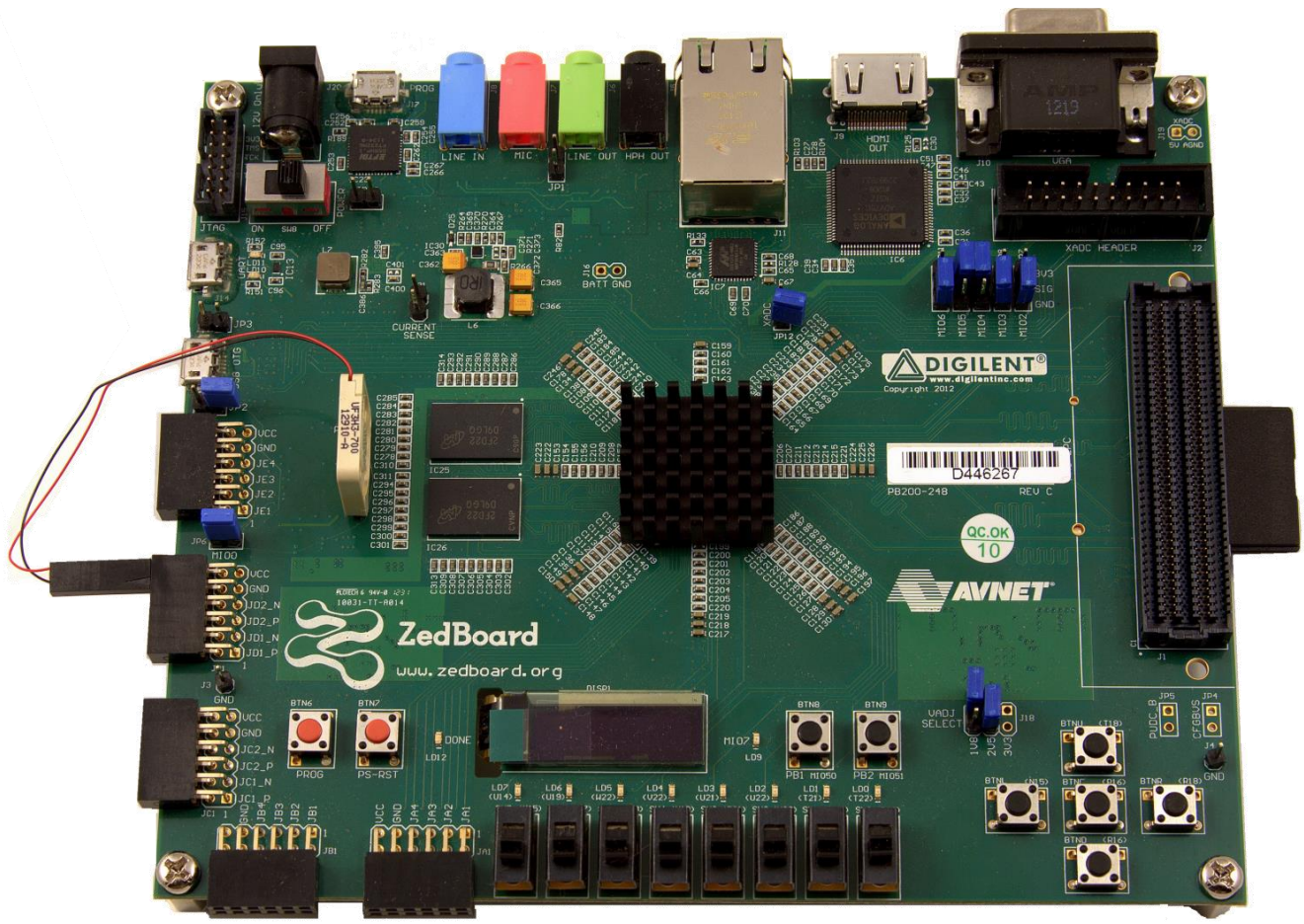

Figure 2 – ZedBoard with Heatsink and Auxiliary Fan attached

3.2 Zynq-7000 USB timing parameter is incompatible with TUSB1210 PHY

Applications Affected

There are no known field failures due to this issue. However, as Zynq moves to production, it is possible based on a datasheet analysis that USB data transfers will fail. The worst-case conditions occur at hot temperatures and low voltage range of the two devices.

Description

The Xilinx Zynq has a hold time requirement for ULPI input data, which is given by $T_{ULPICKD}$ MIN = 1.0 ns. This specification can be found in the *Zynq-7000 AP SoC (XC7Z010 and XC7Z020: DC and AC Switching Characteristics*, DS187 (v1.2) September 12, 2012, as shown below.

Symbol	Description	Min	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs	10.67		ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	1.0		ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs		8.86	ns
$F_{ULPICLK}$	ULPI reference clock frequency	59.97	60.03	MHz

The Texas Instrument's TUSB1210 does not specify the MIN (fastest) Output Delay (T_{DC},T_{DD}) with ULPI Output Clock. This is observed in *TUSB1210 Standalone USB Transceiver Chip Silicon Data Manual*, SLLSE09F, August, 2012, as shown below.

PARAMETER		INPUT CLOCK		OUTPUT CLOCK		UNIT
		MIN	MAX	MIN	MAX	
T_{SC},T_{SD}	Set-up time (control in, 8-bit data in)		3		6	ns
T_{SC},T_{HD}	Hold time (control in, 8-bit data in)	1.5		0		ns
T_{DC},T_{DD}	Output delay (control out, 8-bit data out)		6		9	ns

According to internal sources at TI, this could be as fast as 0.1ns.

This results in a possible 900ps window where data could be lost.

Workaround

The worst-case scenario is when the Zynq needs the full 1.0ns of Hold Time at the same time that the TUSB1210 outputs data at the fastest possible clock-to-output. According to sources at Xilinx and TI, each chip experiences this worst-case potential under high temperature and low-voltage conditions. It may be possible to prevent an issue by maintaining the devices at lower temperatures. It is recommended that ZedBoard not be operated above room temperature for this reason.

For those designing their own boards based on ZedBoard, it is recommended that the ZedBoard TUSB1210 circuitry NOT be copied. Xilinx recommends interfacing Zynq to SMSC USB PHYs. As an example, the Xilinx ZC702 uses the SMSC USB3320 PHY.

As shown in *USB3320 Highly Integrated Full Featured Hi-Speed USB 2.0 ULPI Transceiver Datasheet*, Revision 1.0 (07-14-09), the USB3320 Output Delay shows a MIN = 1.0 ns, which is compatible with Zynq-7000.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
60MHz ULPI Output Clock Note 4.4					
Setup time (STP, data in)	T_{SC}, T_{SD}	Model-specific **REFCLK**	5.0		ns
Hold time (STP, data in)	T_{HC}, T_{HD}	Model-specific **REFCLK**	0.0		ns
Output delay (control out, 8-bit data out)	T_{DC}, T_{DD}	Model-specific **REFCLK**	1.0	3.5	ns

3.3 ZedBoard Resets when Hot-Plugging a Cable

Applications Affected

After ZedBoard is booted, plugging in a USB or Ethernet cable immediately resets the board. This is visible by the blue "DONE" LED going to the off state.

The board may also reset when touching the Ethernet shield, the usb shield, or other metal on the board, including the screws in the mounting holes of the board.

Description

When the ZedBoard is "on" and powered from the included supply there is no reference to earth ground (the system is floating). When a device that references/connects its shield pins to earth-ground is attached using a shielded cable (like HDMI), a reference/connection to earth-ground is established and the ZedBoard may be reset as the board ground stabilizes.

It is also possible for the ZedBoard to reset in response to ESD events, but this is a separate issue from the hot-plugging reset described above.

Workaround

The only way to solve the floating ground issue is to not introduce a new ground reference while the board is on and operating. If hot-plugging is required for your application, a reference to earth-ground can be established prior to powering on the board by either attaching it to a grounded device, or by using a three-prong power supply that provides a ground reference.

All of the ZedBoard's cable connectors (HDMI, USB, and Ethernet) have their shields connected to a "shield ring" within the PCB that is then connected to board ground through a 1Mohm resistor and ESD-suppression cap. Replacing the 1Mohm resistor with a shunt decreases the likelihood of an ESD event causing a board reset. If you are experiencing excessive ESD related resets in your environment, then you have the option of shunting resistor R281 to suppress the problem. Starting in July 2013, shunting R281 will be the default for shipping ZedBoards.

3.4 ZedBoard Routing Does Not Account for Package Delays

Applications Affected

There are no known field failures due to this issue. However, it is listed here for designers referencing the Rev D ZedBoard schematics and layout.

Description

Xilinx document *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* (UG933 v1.6 December 4, 2013) makes several statements related to routing of high-speed circuits (emphasis added):

- All trace lengths must also include the package delay
- DDR signals also require matched trace lengths
- Differential traces should be length matched to ±5 mil if possible

Table 5-9: **DDR Trace Length Match**

Signal Group	LPDDR2	DDR2	DDR3	Comments
DQ/DM to DQS_P/N in data group	±10 ps	±20 ps	±10 ps	
Address/Control to CK_P/N	±10 ps	±25 ps	±10 ps	

- PHYs that support RGMII v2.0 with internal delays (RGMII-ID)
    - Delay skew for DATA[3:0] and CTL to clock delay should be less than ±50 ps including package time

Workaround

No work-around is possible. ZedBoard ships with a -1 speed-grade Zynq device which is capable of a DDR3 interface speed of 533 MHz. The ZedBoard DDR3 has been tested at frequencies higher than this and passed. Ethernet has also been tested and passed. However, for those designers looking to duplicate the ZedBoard design, you should carefully consider what Xilinx specifies in UG933 as well as your own design objectives to determine how best to route your own board.

For those interested in evaluating the package flight times, these can be obtained using the *partgen* utility in the Xilinx tools. From a Xilinx command prompt, use the following command to obtain the flight times for the Zynq device on the ZedBoard:

```
partgen -v xc7z020clg484
```

3.5 ZedBoard DDR3 Single-Ended Trace Impedance Does Not Match UG933 Recommendation

Applications Affected

There are no known field failures due to this issue. However, it is listed here for designers referencing the Rev C ZedBoard schematics and layout.

Description

The ZedBoard DDR3 single-ended PCB traces targeted a 50 ohm impedance. Xilinx document *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide* (UG933 v1.6 December 4, 2013) specifies a 40 ohm impedance:

Table 5-10: **DDR Trace Impedance**

Signal Group	LPDDR2	DDR2	DDR3/3L	Comments
Single-ended	40Ω	50Ω	40Ω	±10% tolerance
Differential	80Ω	100Ω	80Ω	±10% tolerance

Workaround

No work-around is possible. ZedBoard ships with a -1 speed-grade Zynq device which is capable of a DDR3 interface speed of 533 MHz. The ZedBoard DDR3 has been tested at frequencies higher than this and passed. However, for those designers looking to duplicate the ZedBoard design, you should carefully consider what Xilinx specifies in UG933 as well as your own design objectives to determine how best to route your own board.

3.6 The signal enable for the buffer driving the JTAG FMC-TCK signal to the FMC connector is not connected.

Applications Affected

There are no known field failures due to this issue. However, it is listed here for designers referencing the Rev D ZedBoard schematics and layout, and those users that might wish to add the enable signal to their board.

Description

There is an error in the circuit shown on page 2, section C2, of the ZedBoard schematic. In the schematic the enable line for the IC1B, a buffer intended to drive the JTAG TCK signal on the FMC connector if the FMC-PRSNT signal is active, is shown as pin 1 of IC1. The actual enable line for that buffer should be pin 4, which is not connected. As a result pin 4 of the buffer is floating on the board. The buffer seems to be enabled and passing the JTAG clock independent of the presence of an FMC card.

Workaround

Add a wire from IC1 pin 1, the FMC-PRST signal, to IC1 pin 4 to correct the error if functional issues arise.

New Erratum

Any new erratum found will first be posted in the ZedBoard Forums:

http://zedboard.org/forum

Since this document will only be updated periodically, it is recommended that the ZedBoard Forum also be checked for other, recently found erratum.

4 Additional Support

For additional support, please review the discussions and post your questions to the ZedBoard Forum at

http://zedboard.org/forum

You can also contact your local Avnet/Silica FAE for commercial users and Digilent for academic users.

5 Revision History

Date	Version	Revision
26 May 2013	1.0	Initial Version, ZedBoard Rev D
27 Jan 2014	1.1	Added DDR3 trace impedance section
22 Dec 2015	1.2	Added FMC-TCK buffer error section